Abstract of the Disclosure

A programmable logic integrated circuit device has at least one function-specific circuit block (e.g., a parallel multiplier, a parallel barrel shifter, a parallel arithmetic logic unit, etc.) in addition to the usual multiple regions of programmable logic and the usual programmable interconnection circuit resources. To reduce the impact of use of the function-specific block ("FSB") on the general purpose interconnection resources of the device, inputs and/or outputs of the FSB may be coupled relatively directly to a subset of the logic regions. In addition to conserving general purpose interconnect, resources of the logic regions to which the FSB are connected can be used by the FSB to reduce the amount of circuitry that must be dedicated to the FSB. If the FSB is a multiplier, additional features include facilitating accumulation of successive multiplier outputs (using either addition or subtraction and with sign extension if desired) and/or arithmetically combining the outputs of multiple multipliers.